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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,734	11/20/2000	Vincent K. Chan	0100.0100120	7999

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,734	CHAN ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2004 and 20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,12,17 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12,17 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/716734 Attorney's Docket #: 0100.0100120
Filing Date: 11/20/00;

Applicant: Chan et al.

Examiner: Alexander Williams

Applicant's RCE, filed 1/7/04 has been acknowledged.

Applicant's Pre-Amendment, filed 1/20/04, has been acknowledged.

Claims 2, 10, 11, 13-16, 18-20 and 24-27 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3 to 9, 12 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lai et al. (U.S. Patent # 6,236,568 B1) in view of Huang et al. (U.S. Patent # 6,414,385 B1).

For example, in claim 1, Lai et al. (figures 1 to 4) specifically figure 2 show an integrated circuit package **1** comprising: a first substrate **3** having a first surface and a second surface, the first substrate including at least one heat generating circuit **(inherit)** and having a first coefficient of thermal expansion; and a second substrate **5** having at least a first surface and a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled **(by 6)** to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat generating circuit away from the at least one heat-generating circuit; a metallic heat sink **4** thermally coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion; and an external epoxy molding material **8** disposed exterior to the metallic heat sink **(portion along at 8 on the side and under the heat sink 4)** such that the metallic heat sink, the second substrate **5** and the first substrate **3** are encapsulated by the external epoxy molding material **8**. Lai et al. fail to explicitly show an external epoxy molding material disposed exterior to the metallic heat sink such that the metallic heat sink, the second substrate and the first substrate are fully encapsulated by the external epoxy molding material.

Huang t al. is cited for showing a quad flat non-lead package of a semiconductor device. Specifically, Huang et al. (figures 1 to 8) specifically figure 4 discloses an external epoxy molding material **218** disposed exterior to the metallic heat sink **(228 portion within 218 on the active surface of the semiconductor chip 208)** such that the metallic heat sink, the substrate **228** encapsulated by the external epoxy molding material (see column 3, line 59 to column 4, line 29) for the purpose of improve the heat dissipating performance.

3. The integrated circuit package of claim 1, Lao et al.'s coupling between the metallic heat sink and the second substrate is such as to accommodate movement of the metallic heat sink with respect to the second substrate.

4. The Integrated circuit package of claim 2, Lao et al.'s coefficient of thermal expansion of the metallic heat sink is approximately seven times greater than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

5. The integrated circuit package of claim 1, Lao et al. further comprising: an adhesive layer **6** having a first surface and a second surface, the first surface of the adhesive

layer being physically connected to the second surface of the first substrate, the second surface of the adhesive layer being physically connected to the first surface of the second substrate, wherein a thickness of the adhesive layer is less than or equal to approximately one-sixth of a thickness of the first substrate and wherein the adhesive laver functions to thermally couple the first substrate to the second substrate and to position the second Substrate in a fixed relation with respect to the first substrate.

6. The integrated circuit package of claim 1, Lao et al. further comprising: a printed circuit board substrate **2** having at least a first surface, the printed circuit board substrate including at least one conductive trace **22**; an adhesive laver **7** having a first surface and a second surface, the first surface of the adhesive laver being physically connected to the first surface of the printed circuit board substrate, the second surface of the adhesive layer being physically connected to the first surface of the first substrate, wherein the adhesive layer functions to at least position the first substrate in a fixed relation with respect to the printed circuit board substrate; and at least one electrically conductive path connecting the at least one heat-generating circuit to the at least one conductive trace.

7, The Integrated circuit package of claim 6, Lao et al.'s adhesive layer **7** comprises a conductive epoxy (silver paste).

8. The integrated circuit package of claim 6, Lao et al.'s at least one electrically conductive path comprises at least one wire bond **8**.

9. The integrated circuit package of claim 1, Lao et al.'s thickness of the second substrate **5** is greater than a thickness of the first substrate **3**.

12. The integrated circuit package of claim 1, Lao et al.'s first substrate comprises a first semiconductor material and wherein the second substrate comprises one of the first semiconductor material and a second semiconductor material.

17. Lai et al. (figures 1 to 4) specifically figure 2 show an integrated circuit package **1** comprising: a first substrate **3** having a first surface and a second surface, the first substrate including at least one heat-generating circuit and having a first coefficient of thermal expansion, a second substrate **5** having a first surface and a second surface, the second substrate having a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat-generating circuit away from the at least one heat-generating circuit; a printed

circuit board substrate **2** having at least a first surface, the printed circuit board substrate including at least one conductive trace; a first adhesive laver **6** having a first surface and a second surface, the first surface of the first adhesive layer being physically connected to the second surface of the first substrate, the second surface of tile first adhesive layer being physically connected to the first surface of the second substrate, wherein a thickness of the first adhesive laver is less than or equal to approximately one-sixth of a thickness of the first substrate and wherein the first adhesive layer functions to thermally couple the first substrate to the second substrate and to position the second substrate in a fixed relation with respect to tile first substrate; a second adhesive layer **7** having a first surface and a second surface, the first surface of the second adhesive layer being physically connected to the first surface of the printed circuit board substrate, the second surface of the second adhesive laver being physically connected to the first surface of the first substrate, wherein the second adhesive laver functions to at least position the first substrate in a fixed relation with respect to the printed circuit board substrate; at least one electrically conductive path connecting the at least one heat-generating circuit to the at least one conductive trace; a metallic heat sink thermally **4** coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion; and an external epoxy molding material **8** disposed exterior to the metallic heat sink **(portion along at 8 on the side and under the heat sink 4)** such that the metallic heat sink, the second substrate **5** and the first substrate **3** are encapsulated by the external epoxy molding material **8**.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Huang et al.'s fully encapsulated heat sink and semiconductor device to modify Lai's heat sink and device for the purpose of improve the heat dissipating performance.

Claims 21 to 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lai et al. (U.S. Patent # 6,236,568 B1).

For example, in claim 21, Lai et al. (figures 1 to 4) specifically figure 2 show an integrated circuit package **1** comprising: a first substrate **3** having a first surface and a second surface, the first substrate including at least one heat generating circuit **(inherit)** and having a first coefficient of thermal expansion; and a second substrate **5** having at

least a first surface and a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled **(by 6)** to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat generating circuit away from the at least one heat-generating circuit; thermally coupling a metallic heat sink **4** thermally coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion; and an external epoxy molding material **8** disposed exterior to the metallic heat sink **(portion along at 8 on the side and under the heat sink 4)** such that the metallic heat sink, the second substrate **5** and the first substrate **3** are encapsulated by the external epoxy molding material **8**, but fail to explicitly show the method for fabricating an integrated circuit. Huang et al. (figures 1 to 8) specifically figure 4 discloses an external epoxy molding material **218** disposed exterior to the metallic heat sink **(228 portion within 218 on the active surface of the semiconductor chip 208)** such that the metallic heat sink, the substrate **228** encapsulated by the external epoxy molding material (see column 3, line 59 to column 4, line 29) for the purpose of improve the heat dissipating performance. However, it would be obvious to one of ordinary skill in the art to use the teaching of Lao et al.'s heat dissipating structure for an integrated circuit package to form the method for fabricating an integrated circuit of the purpose of preventing the encapsulant to cause a large thermal compressive stress on the integrated circuit chip during the cooling process.

22. The method of claim 21, Lai et al.'s second substrate has a second surface, the integrated circuit package further comprising: a metallic heat sink **4** thermally coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

23. The integrated circuit package of claim 21, Lao et al.'s first substrate comprises a first semiconductor material and wherein the second substrate comprises one of the first semiconductor material and a second semiconductor material.

Therefore, it would have been obvious to one of ordinary skill in the art to use the Huang et l.'s encapsulated heat sink and the teaching of Lai et al.'s heat dissipating structure for an integrated circuit package to form the method for fabricating an

integrated circuit claimed by Applicant of the purpose of preventing the encapsulant to cause a large thermal compressive stress on the integrated circuit chip during the cooling process.

Response

Applicant's arguments filed 1/20/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/712,710,704,712,713,717,720,723,685,686,684,796, 784,786,787,777,778,734,737,738 361/702-704,717,718,715 165/20.3	3/17/03 8/26/03 4/16/04
Other Documentation: foreign patents and literature in 257/712,710,704,712,713,717,720,723,685,686,684,796, 784,786,787,777,778,734,737,738 361/702-704,717,718,715 165/20.3	3/17/03 8/26/03 4/16/04
Electronic data base(s): U.S. Patents EAST	3/17/03 8/26/03 4/16/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1924. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
3/16/04

Alexander Williams
Primary Examiner